Three-Axis, ±2 g/±4 g/±8 g/±16*g* Digital Accelerometer

Preliminary Technical Data

ADXL346

FEATURES

Ultralow power: 25 µA to 145 µA at V_S = 1.8 V (typ)
Power consumption scales automatically with bandwidth
User-selectable resolution
Fixed 10-bit resolution
Full resolution, where resolution increases with *g* range, up to 13-bit resolution at ±16 *g* (maintaining 4 mg/LSB scale factor in all *g* ranges)
32 levels of output data FIFO minimizes host processor load
Tap/double tap detection
Activity/inactivity monitoring
Free-fall detection
4- and 6-position orientation sensing
Supply and I/O voltage range: 1.7 V to 2.75 V
SPI (3 and 4 wire) and I²C digital interfaces
Flexible interrupt modes—any interrupt mappable to either interrupt pin
Measurement ranges selectable via serial command
Bandwidth selectable via serial command
Wide temperature range (−40°C to +85°C)
10,000 *g* shock survival
Pb free/RoHS compliant
Small and thin: 3 mm × 3 mm × 1 mm LGA package

APPLICATIONS

Handsets
Gaming and pointing devices
Personal navigation devices
Hard disk drive (HDD) protection
Fitness equipment
Digital cameras

GENERAL DESCRIPTION

The ADXL346 is a small, thin, low power, three-axis accelerometer with high resolution (13-bit) measurement at up to ±16 *g*. Digital output data is formatted as 16-bit twos complement and is accessible through either a SPI (3- or 4-wire) or I²C digital interface.

The ADXL346 is well suited for mobile device applications. It measures the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (4 mg/LSB) enables measurement of inclination changes as little as 0.25°.

Several special sensing functions are provided. Activity and inactivity sensing detect the presence or lack of motion and if the acceleration on any axis exceeds a user-set level. Tap sensing detects single and double taps. Free-fall sensing detects if the device is falling. These functions can be mapped to one of two interrupt output pins. An integrated 32-level first in, first out (FIFO) buffer can be used to store data to minimize host processor intervention. Both 4- and 6-position orientation sensing are available for 2- and 3-D applications.

Low power modes enable intelligent motion-based power management with threshold sensing and active acceleration measurement at extremely low power dissipation.

The ADXL346 is supplied in a small, thin, 3 mm × 3 mm × 1 mm, 16-lead, plastic package.

FUNCTIONAL BLOCK DIAGRAM

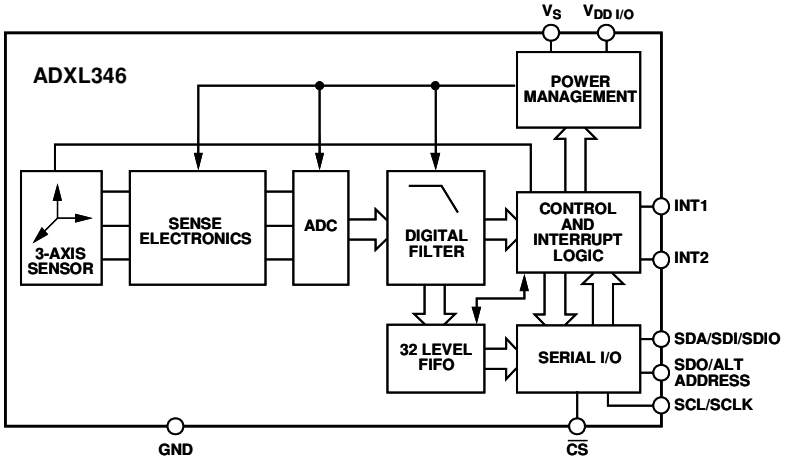

Figure 1.

Rev. PrB

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REVISION HISTORY

4/09 – Revision PrB: Updated Absolute Maximum Ratings table to reflect correct values for the ADXL346.

3/09—Revision PrA: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 1.8 V, $V_{DD\ I/O}$ = 1.8 V, acceleration = 0 *g*, C_S = 1 µF tantalum, C_{IO} = 0.1 µF, unless otherwise noted.

Table 1. Specifications[1]

Parameter	Conditions	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8, ±16		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Inter-Axis Alignment Error			±0.1		Degrees
Cross-Axis Sensitivity[2]			±1		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges	10-bit resolution		10		Bits
±2 *g* Range	Full resolution		10		Bits
±4 *g* Range	Full resolution		11		Bits
±8 *g* Range	Full resolution		12		Bits
±16 *g* Range	Full resolution		13		Bits
SENSITIVITY	Each axis				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±2 *g* 10-bit or full resolution	232	256	286	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±2 *g* 10-bit or full resolution	3.5	3.9	4.3	m*g*/LSB
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±4 *g* 10-bit resolution	116	128	143	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±4 *g* 10-bit resolution	7.0	7.8	8.6	m*g*/LSB
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±8 *g* 10-bit resolution	58	64	71	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±8 *g* 10-bit resolution	14.0	15.6	17.2	m*g*/LSB
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±16 *g* 10-bit resolution	29	32	36	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±16 *g* 10-bit resolution	28.1	31.2	34.3	m*g*/LSB
Sensitivity Change due to Temperature			±0.02		%/°C
0 *g* BIAS LEVEL	Each axis				
0 *g* Output (X_{OUT}, Y_{OUT}, Z_{OUT})		−150	0	+150	m*g*
0 *g* Offset vs. Temperature			<±1		m*g*/°C
NOISE PERFORMANCE					
Noise (x-, y-Axes)	Data rate = 100 Hz, ±2 *g* 10-bit or full resolution		<1		LSB rms
Noise (z-Axis)	Data rate = 100 Hz, ±2 *g* 10-bit or full resolution		<1.5		LSB rms
OUTPUT DATA RATE AND BANDWIDTH	User selectable				
Measurement Rate[3]		6.25		3200	Hz
SELF-TEST	Data rate ≥ 100 Hz				
Output Change in x-Axis		0.15		0.55	*g*
Output Change in y-Axis		−0.15		−0.55	*g*
Output Change in z-Axis		0.20		0.90	*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		1.7	1.8	2.75	V
Interface Voltage Range ($V_{DD\ I/O}$)		1.7	1.8	V_S	V
Supply Current	Data rate > 100 Hz		145	185	µA
Supply Current	Data rate < 10 Hz		25		µA
Standby Mode Leakage Current				10	µA
Turn-On Time[4]	Data rate = 3200 Hz		1.4		ms
TEMPERATURE					
Operating Temperature Range		−40		+85	°C
WEIGHT					
Device Weight			20		mg

[1] All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.
[2] Cross-axis sensitivity is defined as coupling between any two axes.
[3] Bandwidth is half the output data rate.
[4] Turn-on and wake-up times are determined by the user-defined bandwidth. At a 100 Hz data rate, the turn-on and wake-up times are each approximately 11.1 ms. For additional data rates, the turn-on and wake-up times are each approximately τ + 1.1 in milliseconds, where τ is 1/(data rate).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	10,000 *g*
Any Axis, Powered	10,000 *g*
V_S	−0.3 V to +2.75 V
$V_{DD\ I/O}$	−0.3 V to +2.75 V
Digital Pins	−0.3 V to $V_{DD\ I/O}$ + 0.3 V
All Other Pins	−0.3 V to +2.75 V
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
Temperature Range	
Powered	−40°C to +105°C
Storage	−40°C to +105°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	150°C/W	85°C/W	20 mg

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

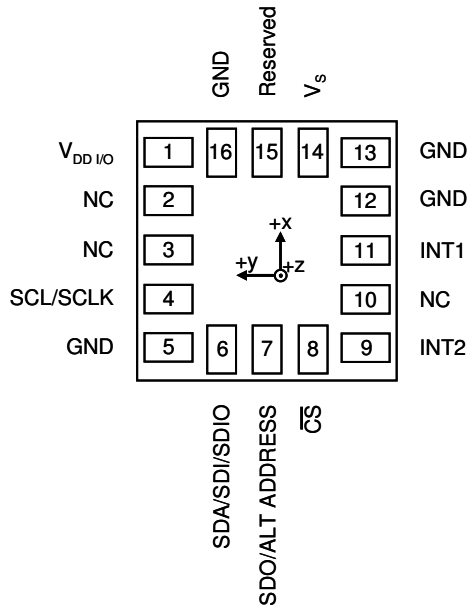


Figure 2. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
2	NC	Not Connected.
3	NC	Not Connected.
4	SCL/SCLK	Serial Communications Clock.
5	GND	Must be connected to ground.
6	SDA/SDI/SDIO	Serial Data (I^2C)/Serial Data Input (SPI 4-Wire)/Serial Data Input and Output (SPI 3-Wire).
7	SDO/ALT ADDRESS	Serial Data Output/Alternate I^2C Address Select.
8	$\overline{CS}$	Chip Select.
9	INT2	Interrupt 2 Output.
10	NC	Not Connected.
11	INT1	Interrupt 1 Output.
12	GND	Must be connected to ground.
13	GND	Must be connected to ground.
14	V_S	Supply Voltage.
15	Reserved	Reserved. This pin must be connected to V_S.
16	GND	Must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

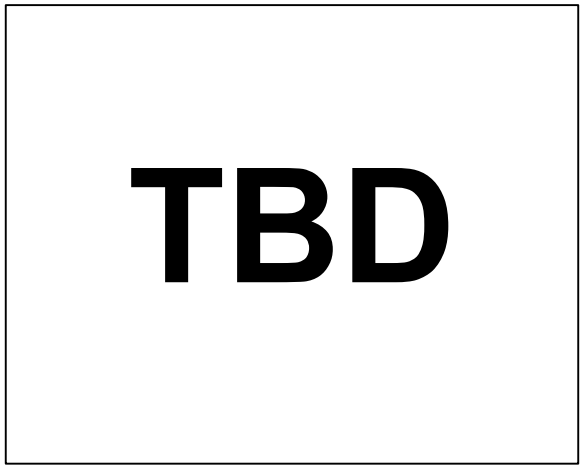


Figure 3.

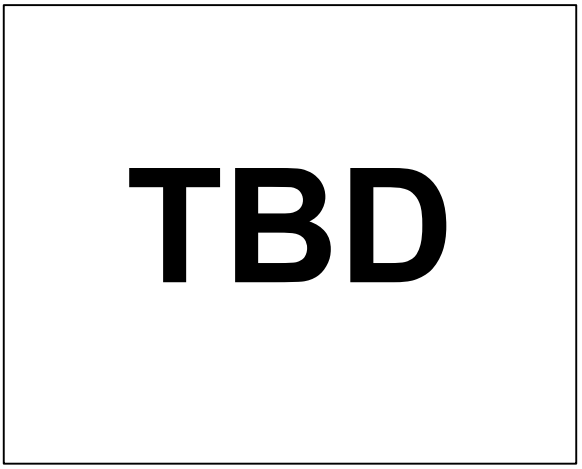


Figure 6.

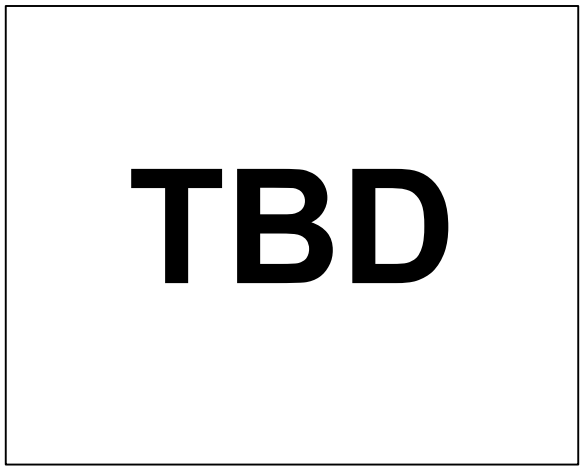


Figure 4.

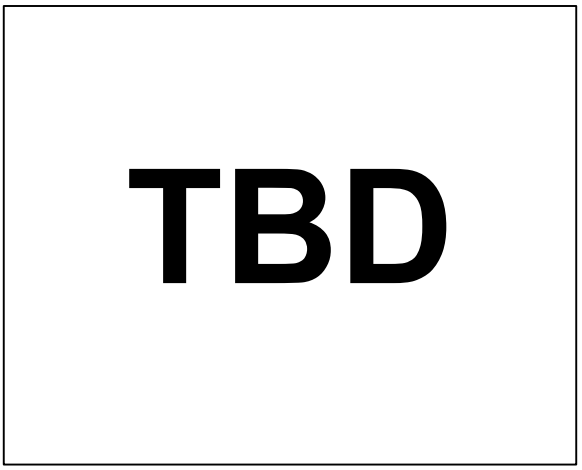


Figure 7.

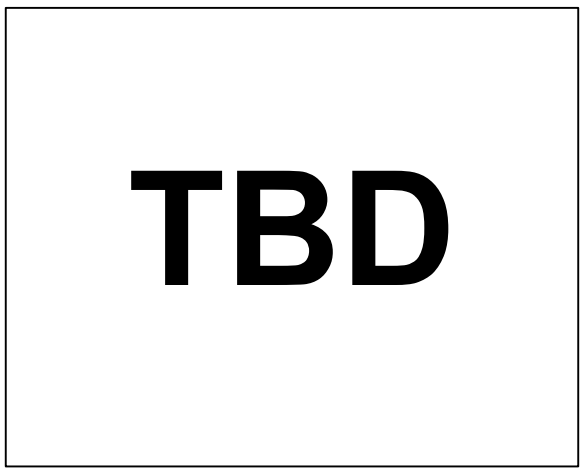


Figure 5.

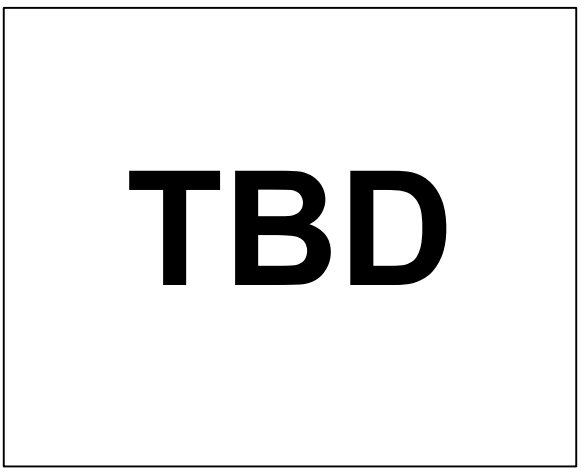
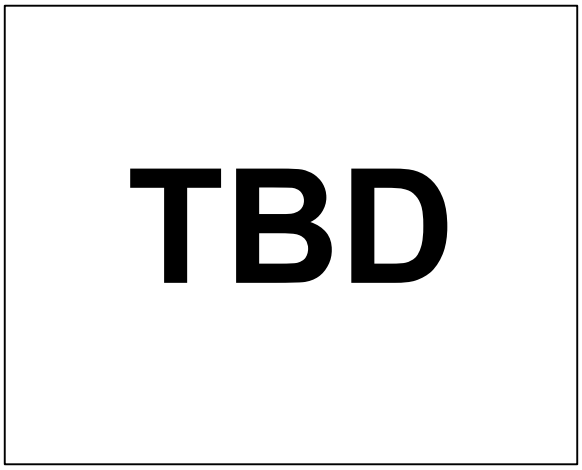


Figure 8.



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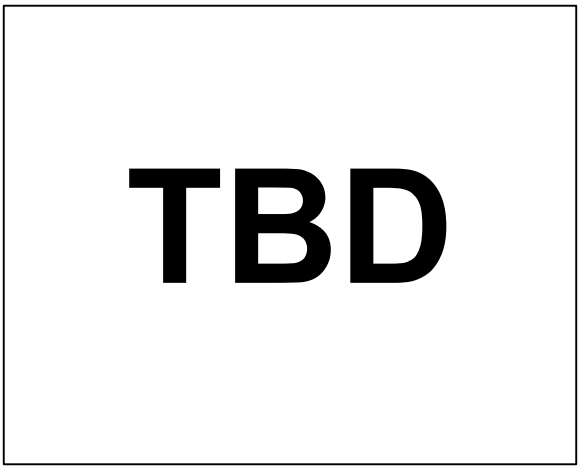
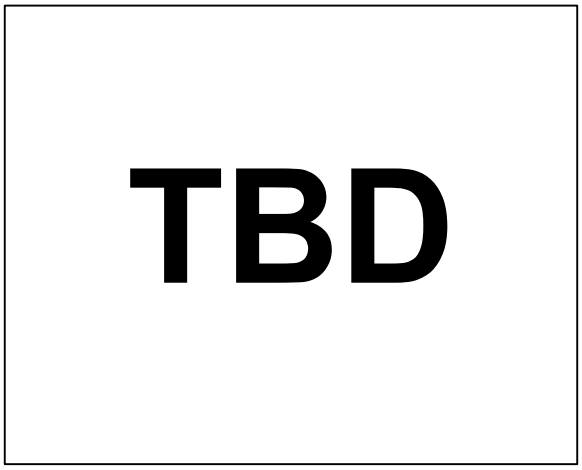


Figure 12.



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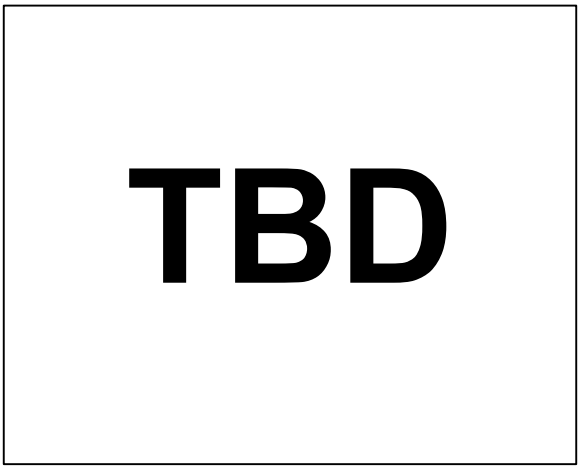

Figure 13.

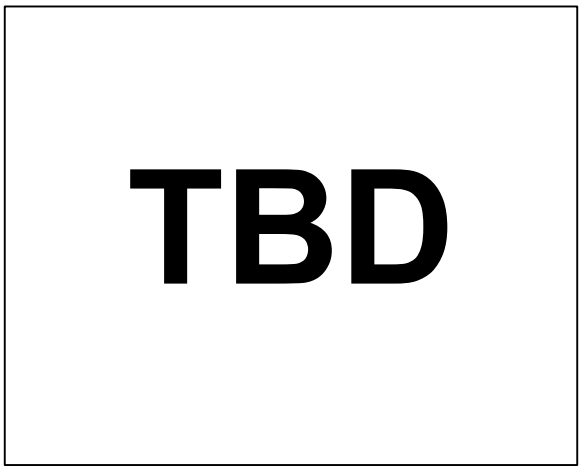

Figure 11.

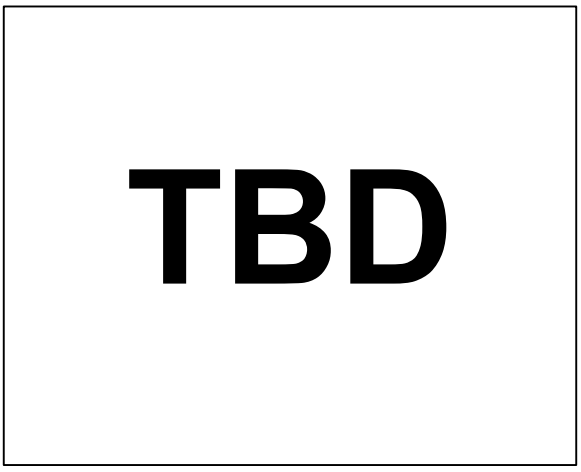

Figure 14.

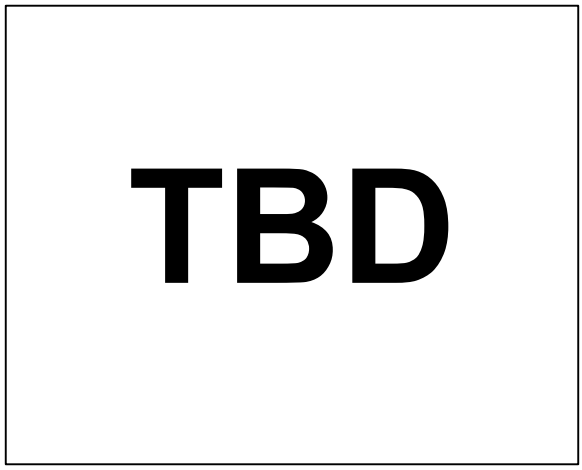

Figure 15.

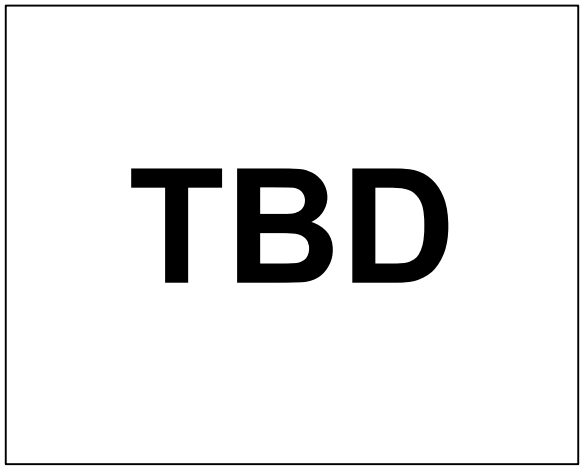

Figure 16.

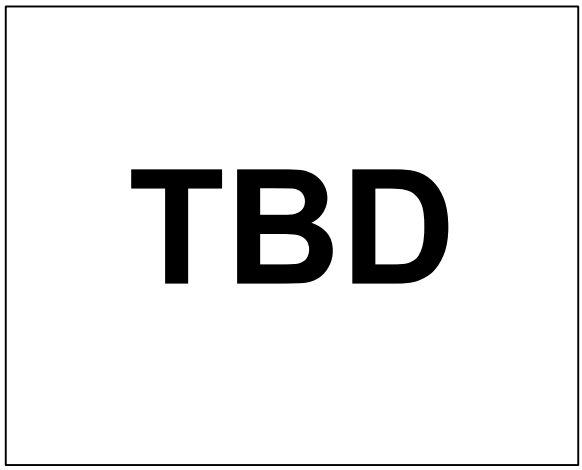

Figure 17.

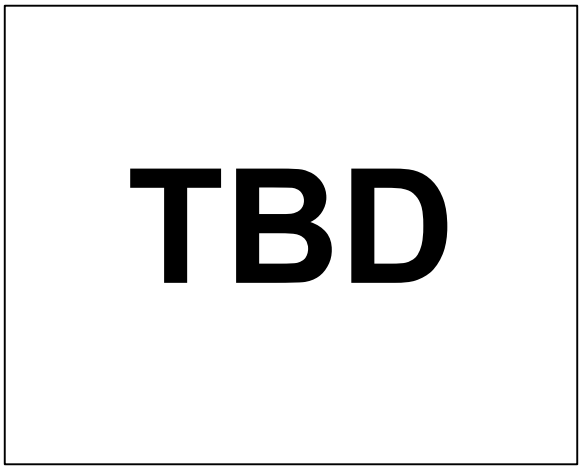

Figure 18.

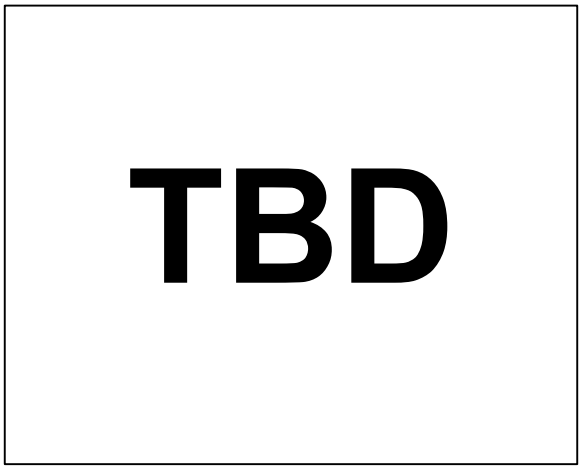

Figure 19.

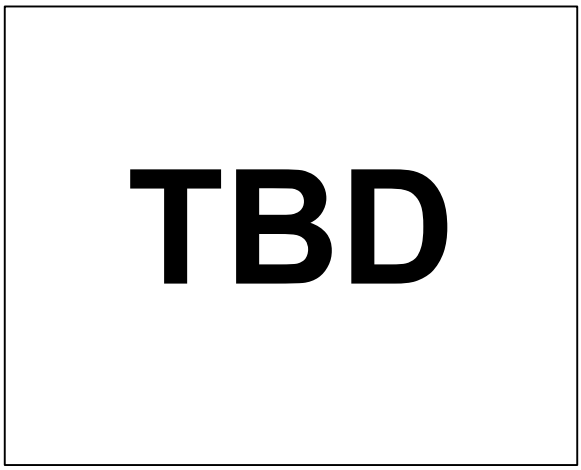

Figure 20.

THEORY OF OPERATION

The ADXL346 is a complete three-axis acceleration measurement system with a selectable measurement range of ±2 *g*, ±4 *g*, ±8 *g*, or ±16 *g*. It measures both dynamic acceleration resulting from motion or shock and static acceleration, such as gravity, which allows it to be used as a tilt sensor.

The sensor is a polysilicon surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the beam and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase-sensitive demodulation is used to determine the magnitude and polarity of the acceleration.

POWER SEQUENCING

Power can be applied to V_S or $V_{DD\ I/O}$ in any sequence without damaging the ADXL346. All possible power-on states are summarized in Table 5. The interface voltage level is set with the interface supply voltage $V_{DD\ I/O}$, which must be present to ensure that the ADXL346 does not create a conflict on the communication bus. For single-supply operation, $V_{DD\ I/O}$ can be the same as the main supply, V_S. Conversely, in a dual-supply application, $V_{DD\ I/O}$ can differ from V_S, as long as V_S is greater than $V_{DD\ I/O}$, to accommodate the desired interface voltage. After V_S is applied, the device enters standby state, where power consumption is minimized and the device waits for $V_{DD\ I/O}$ to be applied and a command to enter measurement state. (This command can be initiated by setting the measure bit in the POWER_CTL register (Address 0x2D).) Clearing the measure bit returns the device to standby state.

Table 5. Power Sequencing

Condition	V_S	$V_{DD\ I/O}$	Description
Power Off	Off	Off	The device is completely off, potential for communication bus conflict.
Bus Enabled	Off	On	No functions are available, but the device will not create conflict on communication bus.
Standby or Measurement	On	On	At power-up, the device is in standby mode, awaiting a command to enter measurement mode, and all sensor functions are off. Once the device is instructed to enter measurement mode, all sensor functions are available.

POWER SAVINGS

Power Modes

The ADXL346 automatically modulates its power consumption in proportion to its output data rate, as shown in Table 6. If additional power savings is desired, a lower power mode is available. In this mode, the internal sampling rate is reduced, allowing for power savings in the 12.5 Hz to 400 Hz data rate range but at the expense of slightly greater noise. To enter lower power mode, set the LOW_POWER bit (Bit 4) in the BW_RATE register (Address 0x2C). The current consumption in low power mode is shown in Table 7 for cases where there is an advantage for using low power mode. The current consumption values shown in Table 6 and Table 7 are for a V_S of 1.8 V. Current will scale linearly with V_S.

Table 6. Current Consumption vs. Data Rate (T_A = 25°C, V_S = 1.8 V, $V_{DD\ I/O}$ = 1.8 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
3200	1600	1111	145
1600	800	1110	90
800	400	1101	145
400	200	1100	145
200	100	1011	145
100	50	1010	145
50	25	1001	90
25	12.5	1000	61
12.5	6.25	0111	41
6.25	3.125	0110	25

Table 7. Current Consumption vs. Data Rate in Low Power Mode (T_A = 25°C, V_S = 1.8 V, $V_{DD\ I/O}$ = 1.8 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
400	200	1100	90
200	100	1011	61
100	50	1010	41
50	25	1001	33
25	12.5	1000	25
12.5	6.25	0111	25

Auto Sleep Mode

Additional power can be saved by having the ADXL346 automatically switch to sleep mode during periods of inactivity. To enable this feature set the THRESH_INACT register (Address 0x25) to an acceleration value that signifies no activity (this value will depend on the application), set TIME_INACT register (Address 0x26) to an appropriate inactivity time period (again, this will depend on the application), and set the AUTO_SLEEP bit and the link bit in the POWER_CTL register (Address 0x2D). Current consumption at the sub-8 Hz data rates used in this mode is typically 25 μA for a V_S of 1.8 V.

Standby Mode

For even lower power operation, standby mode can be used. In standby mode, current consumption is reduced to 10 μA (max). In this mode, no measurements are made and communication with the ADXL346 is limited to single-byte reads or writes. Standby mode is entered by clearing the measure bit (Bit 3) in the POWER_CTL register (Address 0x2D). Placing the device into standby mode preserves the contents of FIFO.

SERIAL COMMUNICATIONS

I²C and SPI digital communications are available. In both cases, the ADXL346 operates as a slave. I²C mode is enabled if the $\overline{CS}$ pin is tied high to $V_{DD\ I/O}$. The $\overline{CS}$ pin should always be tied high to $V_{DD\ I/O}$ or driven by an external controller, as there is no default mode if the $\overline{CS}$ pin is left unconnected. This could result in an inability to communicate with the part. In SPI mode, the $\overline{CS}$ pin is controlled by the bus master. In both SPI and I²C modes of operation, data transmitted from the ADXL346 to the master device should be ignored during writes to the ADXL346.

SPI

For SPI, either 3-wire or 4-wire configuration is possible, as shown in the connection diagrams in Figure 21 and Figure 22. Clearing the SPI bit in the DATA_FORMAT register (Address 0x31) selects 4-wire mode, whereas setting the SPI bit selects 3-wire mode. The maximum SPI clock speed is 5 MHz with 12 pF maximum loading, and the timing scheme follows clock polarity (CPOL) = 1 and clock phase (CPHA) = 1.

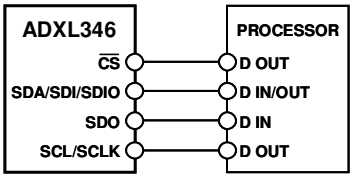

Figure 21. 4-Wire SPI Connection

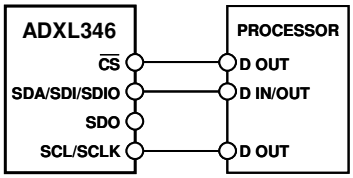

Figure 22. 3-Wire SPI Connection

$\overline{CS}$ is the serial port enable line and is controlled by the SPI master. It must go low at the start of a transmission and back high at the end of a transmission as shown in Figure 23. SCLK is the serial port clock and is supplied by the SPI master. It is stopped high when $\overline{CS}$ is high during a period of no transmission. SDI and SDO are the serial data input and output, respectively. Data should be sampled at the rising edge of SCLK.

To read or write multiple bytes in a single transmission, the multibyte bit, located after the R/W bit in the first byte transfer (MB in Figure 23 to Figure 25), must be set. After the register addressing and the first byte of data, each subsequent set of clock pulses (eight clock pulses) causes the ADXL346 to point to the next register for a read or write. This shifting continues until the clock pulses are ceased and $\overline{CS}$ is deasserted. To perform reads or writes on different, nonsequential registers, $\overline{CS}$ must be deasserted between transmissions and the new register must be addressed separately.

The timing diagram for 3-wire SPI reads or writes is shown in Figure 23. The 4-wire equivalents for SPI reads and writes are shown in Figure 24 and Figure 25, respectively.

Table 8. SPI Timing Specifications
(T_A = 25°C, V_S = 1.8 V, $V_{DD\ I/O}$ = 1.8 V)

Parameter	Limit	Unit	Description
f_{SCLK}	5	MHz max	SPI clock frequency
t_{SCLK}	200	ns min	1/(SPI clock frequency) mark/space ratio for the SCLK input is 40/60 to 60/40
t_{DELAY}	200	ns min	CS Falling edge to SCLK falling edge
t_{QUIET}	200	ns min	SCLK rising edge to CS rising edge
t_S	0.4 × t_{SCLK}	ns min	SCLK low pulse width (space)
t_M	0.4 × t_{SCLK}	ns min	SCLK high pulse width (mark)
t_{SDO}	8	ns max	SCLK falling edge to SDO transition
t_{SETUP}	10	ns min	SDI valid before SCLK rising edge
t_{HOLD}	10	ns min	SDI valid after SCLK rising edge

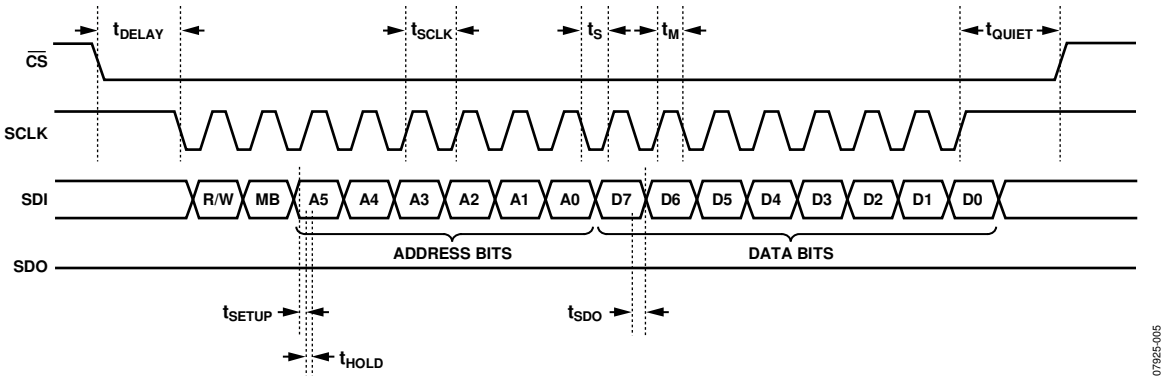

Figure 23. SPI 3-Wire Timing Diagram

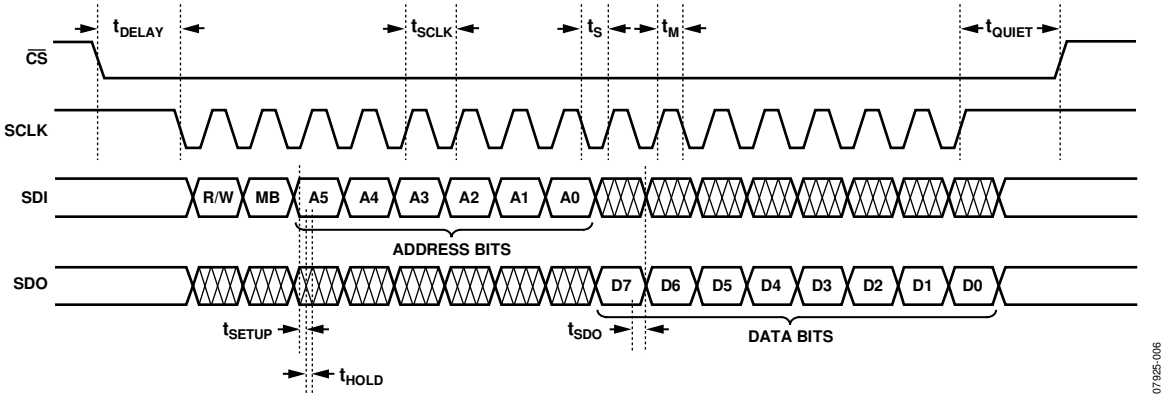

Figure 24. SPI 4-Wire Read Timing Diagram

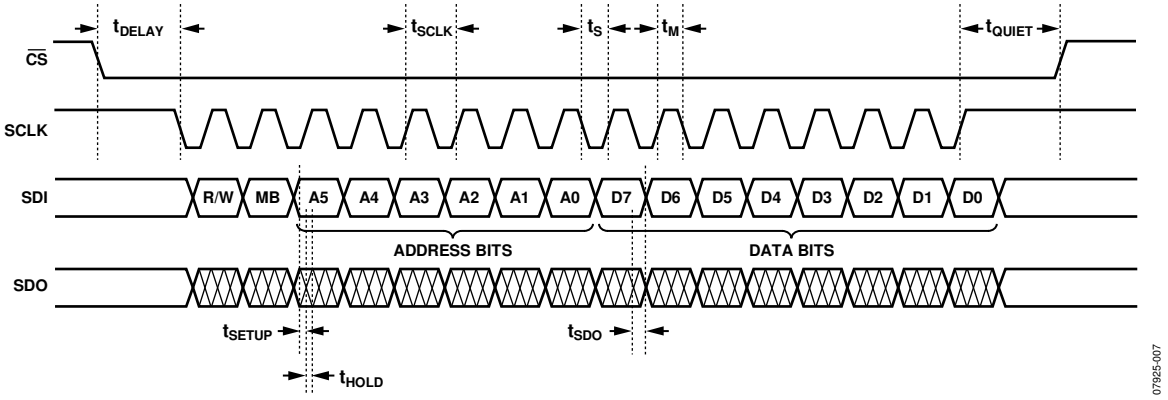

Figure 25. SPI 4-Wire Write Timing Diagram

I²C

With $\overline{CS}$ tied high to $V_{DD\ I/O}$, the ADXL346 is in I²C mode, requiring a simple 2-wire connection as shown in Figure 26. The ADXL346 conforms to *The I²C Bus Specification*, Version 2.1, January 2000, available from Phillips Semiconductor. It supports standard (100 kHz) and fast (400 kHz) data transfer modes. Single- or multiple-byte reads/writes are supported, as shown in Figure 27. With the SDO pin high, the 7-bit I²C address for the device is 0x1D, followed by the R/W bit. This translates to 0x3A for a write, 0x3B for a read. An alternate I²C address of 0x53 (followed by the R/W bit) can be chosen by grounding the SDO pin (Pin 12). This translates to 0xA6 for a write, 0xA7 for a read.

If other devices are connected to the same I²C bus, the nominal operating voltage level of these other devices cannot exceed $V_{DD\ I/O}$ by more than 0.3 V. Pull-up resistors, R_P, should be in the range of 1 kΩ to 20 kΩ.

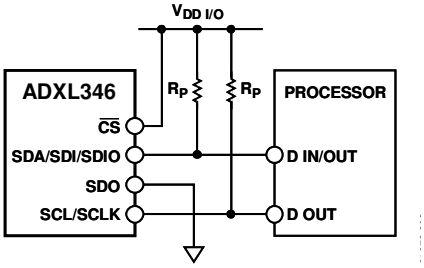

Figure 26. I²C Connection Diagram (Address 0x53)

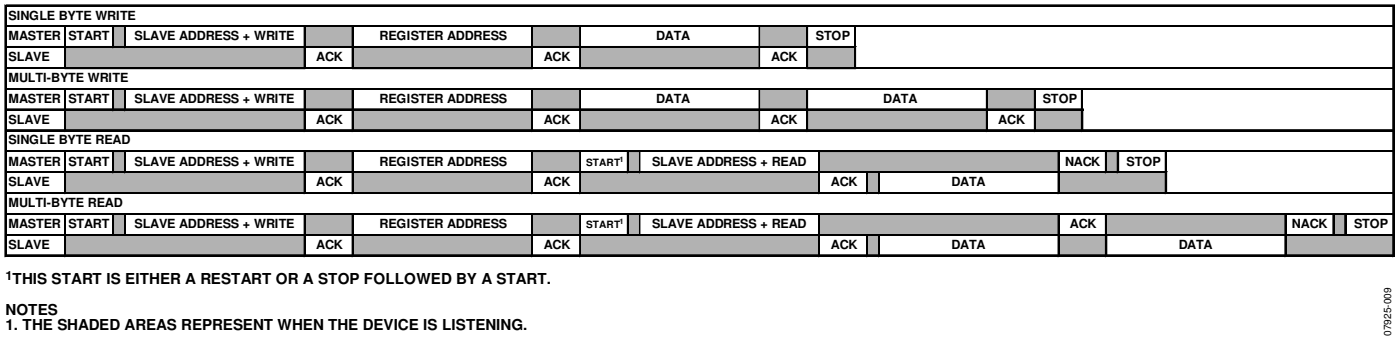

Figure 27. I²C Timing Diagram

INTERRUPTS

The ADXL346 provides two output pins for driving interrupts: INT1 and INT2. Each of the interrupt functions are described in detail in this section. All functions can be used simultaneously, with the only limiting feature being that some functions may need to share interrupt pins. Interrupts are enabled by setting the appropriate bit in the INT_ENABLE register (Address 0x2E) and are mapped to either the INT1 or INT2 pins based on the contents of the INT_MAP register (Address 0x2F). It is recommended that interrupt bits be configured with the interrupts disabled, preventing interrupts from being accidentally triggered during configuration. This can be done by writing a value of 0x00 to the INT_ENABLE register. Clearing interrupts is performed by reading the data registers (Register 0x32 to Register 0x37) until the interrupt condition is no longer valid, for data related interrupts, or reading the INT_SOURCE register (Register 0x30) for the remaining interrupts.

DATA_READY

The DATA_READY bit is set when new data is available and is cleared when no new data is available.

SINGLE_TAP

The SINGLE_TAP bit is set when a single acceleration event that is greater than the value in the THRESH_TAP register (Address 0x1D) occurs for shorter than the time specified in the DUR register (Address 0x21).

DOUBLE_TAP

The DOUBLE_TAP bit is set when two acceleration events that are greater than the value in the THRESH_TAP register occur for shorter than the time specified in the DUR register, with the second tap starting after the time specified by the latent register (Address 0x22) and within the time specified in the window register (Address 0x23). See the Tap Detection section for more details.

Activity

The activity bit is set when acceleration greater than the value stored in the THRESH_ACT register (Address 0x24) is experienced.

Inactivity

The inactivity bit is set when acceleration of less than the value stored in the THRESH_INACT register (Address 0x25) is experienced for longer than the time specified in the TIME_INACT register (Address 0x26). The maximum value for TIME_INACT is 255 sec.

FREE_FALL

The FREE_FALL bit is set when acceleration of less than the value stored in the THRESH_FF register (Address 0x28) is experienced for longer than the time specified in the TIME_FF register (Address 0x29). The FREE_FALL interrupt differs from the inactivity interrupt in that all axes always participate, the timer period is much smaller (1.28 sec maximum), and mode of operation is always dc-coupled.

Watermark

The watermark bit is set when FIFO has filled up to the value stored in the samples bits (Register FIFO_CTL, Address 0x38). The watermark bit is cleared automatically when FIFO is read and the content returns to a value below the value stored in the samples bits.

Overrun

The overrun bit is set when new data replaces unread data. The precise operation of the overrun function depends on the FIFO mode. In bypass mode, the overrun bit is set when new data replaces unread data in the DATAX, DATAY, and DATAZ registers (Register 0x32 to Register 0x37). In all other modes, the overrun bit is set when FIFO is filled. The overrun bit is automatically cleared when the contents of FIFO are read.

FIFO

The ADXL346 contains a 32-level FIFO that can be used to minimize host processor burden. This buffer has four modes: bypass, FIFO, stream, and trigger (see Table 16). Each mode is selected by the settings of the FIFO_MODE bits in the FIFO_CTL register (Address 0x38).

Bypass Mode

In bypass mode, FIFO is not operational and, therefore, remains empty.

FIFO Mode

In FIFO mode, data from x-, y-, and z-axes measurements are stored in FIFO. When FIFO is filled to the level specified in the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set. FIFO continues filling until it is full (32 samples of x-, y-, and z-axes measurements) and then stops collecting data. After FIFO stops collecting data, the device continues to operate; therefore, features like tap detection can still be used after FIFO is full. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the samples bits of the FIFO_CTL register.

Stream Mode

In stream mode, data from the x-, y-, and z-axes measurements are stored in FIFO. When FIFO is filled to the level specified in the samples bits of the FIFO_CTL register, the watermark interrupt is set. FIFO continues filling and holds the latest 32 samples of x-, y-, and z-axes measurements, discarding older data as new data arrives. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the samples bits of the FIFO_CTL register.

Trigger Mode

In trigger mode, FIFO fills and holds the latest 32 samples of x-, y-, and z-axes measurements. Once a trigger event occurs and an interrupt is sent to the INT1 or INT2 pin (determined by the trigger bit in the FIFO_CTL register), FIFO keeps the last n samples (where n is the value specified by the samples bits in the FIFO_CTL register) and then operates in FIFO mode, collecting new samples only when FIFO is not full. Additional trigger events cannot be recognized until trigger mode is reset. This can be done by setting the device to bypass mode, reading the FIFO_STATUS register, and then setting the device back to trigger mode. The FIFO data should be read first because placing the device into bypass mode clears FIFO.

Retrieving Data from FIFO

FIFO data is read through the DATAX, DATAY, and DATAZ registers (Register 0x32 to Register 0x37). When the FIFO is in FIFO, stream, or trigger mode, reads to the DATAX, DATAY, and DATAZ registers read data stored in the FIFO. Each time data is read from the FIFO, the oldest x-, y-, and z-axes data are placed into the DATAX, DATAY and DATAZ registers.

If a single-byte read operation is performed, the remaining bytes of data for the current FIFO sample are lost. Therefore, all axes of interest should be read in a burst (or multibyte) read operation. To ensure that the FIFO has completely popped (that is, that new data has completely moved into the DATAX, DATAY, and DATAZ registers), there must be at least 5 µs between the end of reading the data registers, signified by the transition to Register 0x38 from Register 0x37 or the $\overline{CS}$ pin going high, and the start of a new read of the FIFO or a read of the FIFO_STATUS register (Address 0x39). For SPI operation at 1.5 MHz or lower, the register addressing portion of the transmission is a sufficient delay to ensure that the FIFO has completely popped. For SPI operation greater than 1.5 MHz, it is necessary to deassert the $\overline{CS}$ pin to ensure a total delay of 5 µs; otherwise, the delay will not be sufficient. The total delay necessary for 5 MHz operation is at most 3.4 µs. This is not a concern when using I^2C because the communication rate is low enough to ensure a sufficient delay between FIFO reads.

SELF-TEST

The ADXL346 incorporates a self-test feature that effectively tests its mechanical and electronic systems simultaneously. When the self-test function is enabled (via the SELF_TEST bit in the DATA_FORMAT register, Address 0x31), an electrostatic force is exerted on the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and it is additive to the acceleration experienced by the device. This added electrostatic force results in an output change in the x-, y-, and z-axes. Because the electrostatic force is proportional to V_S^2, the output change varies with V_S.

The self-test feature of the ADXL346 exhibits a bimodal behavior that depends on which phase of the clock self-test is enabled. However, the limits shown in Table 1 and Table 9 to Table 12 are valid for both potential values. Use of the self-test feature at data rates less than 100 Hz may yield values outside these limits. Therefore, the part should be placed into a data rate of 100 Hz or greater when using self-test.

Table 9. Self-Test Output in LSB for ±2 *g* and Full Resolution

	V_S = 1.8 V			V_S = 2.5 V		
Axis	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
X	+40		+135	+80		+260
Y	−40		−135	−80		−260
Z	+60		+220	+120		+420

Table 10. Self-Test Output in LSB for ±4 *g* and 10-Bit Resolution

	V_S = 1.8 V			V_S = 2.5 V		
Axis	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
X	+20		+70	+40		+130
Y	−20		−70	−40		−130
Z	+30		+110	+60		+210

Table 11. Self-Test Output in LSB for ±8 *g* and 10-Bit Resolution

	V_S = 1.8 V			V_S = 2.5 V		
Axis	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
X	+10		+35	+20		+65
Y	−10		−35	−20		−65
Z	+15		+55	+30		+105

Table 12. Self-Test Output in LSB for ±16 *g* and 10-Bit Resolution

	V_S = 1.8 V			V_S = 2.5 V		
Axis	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
X	+5		+18	+10		+33
Y	−5		−18	−10		−33
Z	+7		+28	+15		+53

REGISTER MAP

Table 13. Register Map

Address					
Hex	**Dec**	**Name**	**Type**	**Reset Value**	**Description**
0	0	DEVID	R	11100101	Device ID.
1 to 1C	1 to 28	Reserved			Reserved. Do not access.
1D	29	THRESH_TAP	R/W	00000000	Tap threshold.
1E	30	OFSX	R/W	00000000	X-axis offset.
1F	31	OFSY	R/W	00000000	Y-axis offset.
20	32	OFSZ	R/W	00000000	Z-axis offset.
21	33	DUR	R/W	00000000	Tap duration.
22	34	LATENT	R/W	00000000	Tap latency.
23	35	WINDOW	R/W	00000000	Tap window.
24	36	THRESH_ACT	R/W	00000000	Activity threshold.
25	37	THRESH_INACT	R/W	00000000	Inactivity threshold.
26	38	TIME_INACT	R/W	00000000	Inactivity time.
27	39	ACT_INACT_CTL	R/W	00000000	Axis enable control for activity and inactivity detection.
28	40	THRESH_FF	R/W	00000000	Free-fall threshold.
29	41	TIME_FF	R/W	00000000	Free-fall time.
2A	42	TAP_AXES	R/W	00000000	Axis control for tap/double tap.
2B	43	ACT_TAP_STATUS	R	00000000	Source of tap/double tap.
2C	44	BW_RATE	R/W	00001010	Data rate and power mode control.
2D	45	POWER_CTL	R/W	00000000	Power saving features control.
2E	46	INT_ENABLE	R/W	00000000	Interrupt enable control.
2F	47	INT_MAP	R/W	00000000	Interrupt mapping control.
30	48	INT_SOURCE	R	00000010	Source of interrupts.
31	49	DATA_FORMAT	R/W	00000000	Data format control.
32	50	DATAX0	R	00000000	X-Axis Data 0.
33	51	DATAX1	R	00000000	X-Axis Data 1.
34	52	DATAY0	R	00000000	Y-Axis Data 0.
35	53	DATAY1	R	00000000	Y-Axis Data 1.
36	54	DATAZ0	R	00000000	Z-Axis Data 0.
37	55	DATAZ1	R	00000000	Z-Axis Data 1.
38	56	FIFO_CTL	R/W	00000000	FIFO control.
39	57	FIFO_STATUS	R	00000000	FIFO status.
3A	58	TAP_SIGN	R	00000000	Sign and source for tap/double tap
3B	59	ORIENT_CONF	R/W	00000000	Orientation configuration
3C	60	ORIENT	R	00000000	Orientation status

REGISTER DEFINITIONS

Register 0x00—DEVID (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	0	1

The DEVID register holds a fixed device ID code of 0xE5 (345 octal).

Register 0x1D—THRESH_TAP (Read/Write)

The THRESH_TAP register is eight bits and holds the threshold value for tap interrupts. The data format is unsigned, so the magnitude of the tap event is compared with the value in THRESH_TAP. The scale factor is 62.5 mg/LSB (that is, 0xFF = +16 *g*). A value of 0 may result in undesirable behavior if tap/double tap interrupts are enabled.

Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write)

The OFSX, OFSY, and OFSZ registers are each eight bits and offer user-set offset adjustments in twos compliment format with a scale factor of 15.6 mg/LSB (that is, 0x7F = +2 g).

Register 0x21—DUR (Read/Write)

The DUR register is eight bits and is an unsigned time value representing the maximum time that an event must be above the THRESH_TAP threshold to qualify as a tap event. The scale factor is 625 µs/LSB. A value of 0 disables the tap/double tap functions.

Register 0x22—Latent (Read/Write)

The latent register is eight bits and is an unsigned time value representing the wait time from the detection of a tap event to the start of the time window (defined by the window register) that a possible second tap event can be detected. The scale factor is 1.25 ms/LSB. A value of 0 disables the double tap function.

Register 0x23—Window (Read/Write)

The window register is eight bits and is an unsigned time value representing the amount of time after the expiration of the latency time (determined by the latent register) during which a second valid tap can begin. The scale factor is 1.25 ms/LSB. A value of 0 disables the double tap function.

Register 0x24—THRESH_ACT (Read/Write)

The THRESH_ACT register is eight bits and holds the threshold value for detecting activity. The data format is unsigned, so the magnitude of the activity event is compared with the value in the THRESH_ACT register. The scale factor is 62.5 mg/LSB. A value of 0 may result in undesirable behavior if the activity interrupt is enabled.

Register 0x25—THRESH_INACT (Read/Write)

The THRESH_INACT register is eight bits and holds the threshold value for detecting inactivity. The data format is unsigned, so the magnitude of the inactivity event is compared with the value in the THRESH_INACT register. The scale factor is 62.5 mg/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

Register 0x26—TIME_INACT (Read/Write)

The TIME_INACT register is eight bits and is an unsigned time value representing the amount of time that acceleration must be less than the value in the THRESH_INACT register for inactivity to be declared. The scale factor is 1 sec/LSB. Unlike the other interrupt functions, which use unfiltered data (see the Threshold section), the inactivity function uses filtered output data. At least one output sample must be generated for the inactivity interrupt to be triggered. This results in the function appearing unresponsive if the TIME_INACT register is set with a value less than the time constant of the output data rate. A value of 0 results in an interrupt when the output data is less than the value in the THRESH_INACT register.

Register 0x27—ACT_INACT_CTL (Read/Write)

D7 D3	D6 D2	D5 D1	D4 D0
ACT ac/dc INACT ac/dc	ACT_X enable INACT_X enable	ACT_Y enable INACT_Y enable	ACT_Z enable INACT_Z enable

ACT_x Enable Bits and INACT_x Enable Bits

A setting of 1 enables x-, y-, or z-axis participation to detect activity or inactivity. A setting of 0 excludes the selected axis from participation. If all of the axes are excluded, the function is disabled.

ACT AC/DC and INACT AC/DC Bits

A setting of 0 selects dc-coupled operation, and a setting of 1 enables ac-coupled operation. In dc-coupled operation, the current acceleration magnitude is compared directly with THRESH_ACT and THRESH_INACT to determine whether activity or inactivity is detected.

In ac-coupled operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value, and if the magnitude of the difference exceeds THRESH_ACT, the device triggers an activity interrupt.

Similarly, in ac-coupled operation for inactivity detection, a reference value is used for comparison and is updated whenever the device exceeds the inactivity threshold. Once the reference value is selected, the device compares the magnitude of the difference between the reference value and the current acceleration with THRESH_INACT. If the difference is less than the value in THRESH_INACT for the time in TIME_INACT, the device is considered inactive and the inactivity interrupt is triggered.

Register 0x28—THRESH_FF (Read/Write)

The THRESH_FF register is eight bits and holds the threshold value for free-fall detection. The data format is unsigned. The root-sum-square (RSS) value of all axes is calculated and compared with the value in THRESH_FF to determine if a free-fall event occurred. The scale factor is 62.5 mg/LSB. A value 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 300 mg and 600 mg (0x05 to 0x09) are recommended.

Register 0x29—TIME_FF (Read/Write)

The TIME_FF register is eight bits and stores an unsigned time value representing the minimum time that the RSS value of all axes must be less than THRESH_FF to generate a free-fall interrupt. The scale factor is 5 ms/LSB. A value of 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 100 ms to 350 ms (0x14 to 0x46) are recommended.

Register 0x2A—TAP_AXES (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Suppress	TAP_X enable	TAP_Y enable	TAP_Z enable

TAP_x Enable Bits

A setting of 1 in the TAP_X enable, TAP_Y enable, or TAP_Z enable bit enables x-, y-, or z-axis participation in tap detection. A setting of 0 excludes the selected axis from participation in tap detection.

Suppress Bit

Setting the suppress bit suppresses double tap detection if acceleration greater than the value in THRESH_TAP is present between taps. See the Tap Detection section for more details.

Register 0x2B—ACT_TAP_STATUS (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
X	ACT_X source	ACT_Y source	ACT_Z source	Asleep	TAP_X source	TAP_Y source	TAP_Z source

ACT_x Source and TAP_x Source Bits

These bits indicate the first axis involved in a tap or activity event. A setting of 1 corresponds to involvement in the event, and a setting of 0 corresponds to no involvement. When new data is available, these bits are not cleared but are overwritten by the new data. The ACT_TAP_STATUS register should be read before clearing the interrupt. Disabling an axis from participation clears the corresponding source bit when the next activity or tap/double tap event occurs.

Asleep Bit

A setting of 1 indicates that the part is asleep. A setting of 0 indicates that the part is not asleep. See the Register 0x2D—POWER_CTL (Read/Write) section for more information on auto sleep mode.

Register 0x2C—BW_RATE (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	LOW_POWER	Rate			

LOW_POWER Bit

A setting of 0 selects normal operation, and a setting of 1 chooses reduced power operation, which has somewhat higher noise (see the Power Modes section for details).

Rate Bits

These bits select the device bandwidth and output data rate (see Table 6 and Table 7 for details). The default value is 0x0A, which translates to a 100 Hz output data rate. An output data rate should be selected that is appropriate for the communication protocol and frequency selected. Selecting too high of an output data rate with a low communication speed results in samples being discarded.

Register 0x2D—POWER_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	

Link Bit

A setting of 1 with both the activity and inactivity functions enabled delays the start of the activity function until inactivity is detected. Once activity is detected, inactivity detection begins and prevents the detection of activity. This bit serially links the activity and inactivity functions. When this bit is set to 0, the inactivity and activity functions are concurrent. Additional information can be found in the Link Mode section.

AUTO_SLEEP Bit

A setting of 1 sets the ADXL346 to switch to sleep mode when inactivity is detected (that is, when acceleration has been below the THRESH_INACT value for at least the time indicated by TIME_INACT) and the link bit is set. A setting of 0 disables automatic switching to sleep mode. See the description of the sleep bit in this section for further information.

Measure Bit

A setting of 0 places the part into standby mode, and a setting of 1 places the part into measurement mode. The ADXL346 powers up in standby mode with minimum power consumption.

Sleep Bit

A setting of 0 puts the part into a normal mode of operation, and a setting of 1 places the part into sleep mode. Sleep mode suppresses DATA_READY, stops transmission of data to FIFO, and switches the sampling rate to one specified by the wakeup bits. In sleep mode, only the activity function can be used.

When clearing the link, AUTO_SLEEP, or sleep bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the link, AUTO_SLEEP, or sleep bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Wakeup Bit

This bit controls the frequency of readings in sleep mode as described in Table 14.

Table 14. Frequency of Readings in Sleep Mode

Setting		
D1	**D0**	**Frequency (Hz)**
0	0	8
0	1	4
1	0	2
1	1	1

Register 0x2E—INT_ENABLE (Read/Write)

D7	**D6**	**D5**	**D4**
D3	**D2**	**D1**	**D0**
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
Inactivity	FREE_FALL	Watermark	Overrun

Setting bits with a value of 1 in this register enables their respective functions to generate interrupts, whereas a value of 0 prevents the functions from generating interrupts. The DATA_READY, watermark, and overrun bits only enable the interrupt output; the functions are always enabled. It is recommended that interrupts be configured before enabling their outputs.

Register 0x2F—INT_MAP (Read/Write)

D7	**D6**	**D5**	**D4**
D3	**D2**	**D1**	**D0**
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
Inactivity	FREE_FALL	Watermark	Overrun

Any bits set to 0 in this register send their respective interrupts to the INT1 pin, whereas bits set to 1 send their respective interrupts to the INT2 pin. All selected interrupts for a given pin are OR'ed.

Register 0x30—INT_SOURCE (Read Only)

D7	**D6**	**D5**	**D4**
D3	**D2**	**D1**	**D0**
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
Inactivity	FREE_FALL	Watermark	Overrun

Bits set to 1 in this register indicate that their respective functions have triggered, whereas a value of 0 indicates that the corresponding event has not occurred. The DATA_READY, watermark, and overrun bits are always set if corresponding events occur, regardless of the INT_ENABLE register settings, and are cleared by reading data from the DATAX, DATAY, and DATAZ registers. The DATA_READY and watermark bits may require multiple reads, as indicated in the FIFO mode descriptions in the FIFO section. Other bits, and corresponding interrupts, are cleared by reading the INT_SOURCE register.

Register 0x31—DATA_FORMAT (Read/Write)

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SELF_TEST	SPI	INT_INVERT	X	FULL_RES	Justify	Range	

The DATA_FORMAT register controls the presentation of data to Register 0x32 through Register 0x37. All data, except that for the ±16 *g* range, must be clipped to avoid rollover.

SELF_TEST Bit

A setting of 1 applies a self-test force to the sensor, causing a shift in the output data. A value of 0 disables the self-test force.

SPI Bit

A value of 1 sets the device to 3-wire SPI, and a value of 0 sets the device to 4-wire SPI.

INT_INVERT Bit

A value of 0 sets the interrupts to active high, and a value of 1 sets the interrupts to active low.

FULL_RES Bit

When this bit is set with a value of 1, the device is in full resolution mode, where the output resolution increases with the *g* range set by the range bits to maintain a 4 mg/LSB scale factor. When the FULL_RES bit is set to 0, the device is in 10-bit mode and the range bits determine the maximum *g* range and scale factor.

Justify Bit

A setting of 1 selects left (MSB) justified mode, and a setting of 0 chooses right justified mode with sign extension.

Range Bits

These bits set the *g* range as described in Table 15.

Table 15. *g* Range Setting

Setting		
D1	**D0**	***g* Range**
0	0	±2 *g*
0	1	±4 *g*
1	0	±8 *g*
1	1	±16 *g*

Register 0x32 to Register 0x37—DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, DATAZ1 (Read Only)

These six bytes (Register 0x32 to Register 0x37) are eight bits each and hold the output data for each axis. Register 0x32 and Register 0x33 hold the output data for the x-axis, Register 0x34 and Register 0x35 hold the output data for the y-axis, and Register 0x36 and Register 0x37 hold the output data for the z-axis. The output data is twos complement, with DATAx0 as the least significant byte and DATAx1 as the most significant byte. The DATA_FORMAT register (Address 0x31) controls the format of the data. It is recommended that a burst read of all of the registers be performed to prevent the change of data between reads of sequential registers.

Register 0x38—FIFO_CTL (Read/Write)

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FIFO_MODE		Trigger	Samples				

FIFO_MODE Bits

The settings of these bits correspond to the FIFO mode, as described in Table 16.

Trigger Bit

A value of 0 sets the trigger event of trigger mode to be linked to INT1, and a value of 1 sets the trigger event to be linked to INT2.

Samples Bits

The function of these bits depends on the FIFO mode selected (see Table 17). Entering a value of 0 in the samples bits immediately sets the watermark status bit in the INT_SOURCE register, regardless of which FIFO mode is selected. Undesirable operation may occur if a value of 0 is used for the samples bits when trigger mode is used.

Table 16. FIFO Modes

Setting			
D7	**D6**	**Mode**	**Function**
0	0	Bypass	FIFO is bypassed.
0	1	FIFO	FIFO collects up to 32 values and then stops collecting data, collecting new data only when FIFO is not full.
1	0	Stream	FIFO holds the last 32 data values. Once FIFO is full, the oldest data is lost as it is replaced with newer data.
1	1	Trigger	When triggered by the trigger bit, FIFO holds the last data samples before the trigger event and then continues to collect data until full. New data is collected only when FIFO is not full.

Table 17. SAMPLES Functions

FIFO Mode	Samples Function
Bypass	None.
FIFO	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Stream	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Trigger	Specifies how many FIFO samples before the trigger event are retained in the FIFO buffer.

0x39—FIFO_STATUS (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_TRIG	X	Entries					

FIFO_TRIG Bit

A 1 corresponds to a trigger event occurring, and a 0 means that a FIFO trigger event has not occurred.

Entries Bits

These bits report how many data values are stored in FIFO. Access to collect the data from FIFO is provided through the DATAX, DATAY, and DATAZ registers. FIFO reads must be done in burst or multibyte mode because each FIFO level is cleared after any read, single- or multibyte, of FIFO. FIFO stores a maximum of 32 entries, which equates to a maximum of 33 entries available at any given time due to the fact that an additional entry is available at the output filter of the device.

Register 0x3A—TAP_SIGN (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
0	XSIGN	YSIGN	ZSIGN	0	XTAP	YTAP	ZTAP

xSIGN Bits

These bits indicate the sign of the first axis involved in a tap event. A setting of 1 corresponds to acceleration in the negative direction and a setting of 0 corresponds to acceleration in the positive direction. These bits will only update when a new tap/double tap event is detected and only those axes enabled TAP_AXES register will be updated. The TAP_SIGN register should be read before clearing the interrupt. See the Tap Sign section for more details.

xTAP Bits

These bits indicate the first axis involved in a tap event. A setting of 1 corresponds to involvement in the event, and a setting of 0 corresponds to no involvement. When new data is available, these bits are not cleared but are overwritten by the new data. The TAP_SIGN register should be read before clearing the interrupt. Disabling an axis from participation clears the corresponding source bit when the next tap/double tap event occurs.

Register 0x3B—ORIENT_CONF (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	Deadzone			0	Divisor		

Deadzone Bits

These bits determine the region between two adjacent orientations where the orientation is considered invalid and is not updated. A value of zero may result in undesirable behavior when the orientation is close to the bisector between two adjacent regions. The deadzone angle is determined by these bits is shown in Table 18. See the Orientation Sensing section for more details.

Divisor Bits

These bits set the depth of the filter used to low-pass filter the measured acceleration for stable orientation sensing. The divisor length is determined by these bits is shown in Table 18. See the Orientation Sensing section for more details.

Table 18. Deadzone and Divisor codes

Decimal	Binary	Deadzone angle [°]	Divisor length
0	000	0.0	2
1	001	3.6	4
2	010	7.2	8
3	011	10.8	16
4	100	14.4	32
5	101	18.0	64
6	110	21.6	128
7	111	25.2	256

Register 0x3C—ORIENT (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
0	V2	2D_ORIENT		V3	3D_ORIENT		

Vx Bits

These bits show the validity of the 2-D (V2) or 3-D (V3) orientation. A value of 1 corresponds to the orientation being valid. A value of 0 means that the orientation is invalid, as the current orientation is in the deadzone.

xD_ORIENT Bits

These bits represent the current 2-D (2D_ORIENT) and 3-D (3D_ORIENT) orientation of the accelerometer. Orientation values are shown in Table 19 and Table 20. See the Orientation Sensing section for more details

Changing the value in the BW_RATE register will cause the orientation sensing filter to be cleared and the function to reset.

Table 19. 2-D orientation codes

Decimal	Binary	Orientation	Dominant Axis
0	000	Portrait Positive	+X
1	001	Portrait Negative	-X
2	010	Landscape Positive	+Y
3	011	Landscape Negative	-Y

Table 20. 3-D orientation codes

Decimal	Binary	Orientation	Dominant Axis
3	011	Front	+X
4	100	Back	-X
2	010	Right	+Y
5	101	Left	-Y
1	001	Top	+Z
6	110	Bottom	-Z

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

A 1 µF tantalum capacitor (C_S) at V_S and a 0.1 µF ceramic capacitor (C_{IO}) at $V_{DD\ I/O}$ placed close to the ADXL346 supply pins is used for testing and recommended to adequately decouple the accelerometer from noise on the power supply. If additional decoupling is necessary, a resistor or ferrite bead, no larger than 100 Ω, in series with V_S may be helpful. Additionally, increasing the bypass capacitance on V_S to a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic may also improve noise.

Care should be taken to ensure that the connection from the ADXL346 ground to the power supply ground has low impedance because noise transmitted through ground has an effect similar to noise transmitted through V_S. It is recommended that V_S and $V_{DD\ I/O}$ be separate supplies to minimize digital clocking noise on the V_S supply. If this is not possible, additional filtering of the supplies as previously mentioned may be necessary.

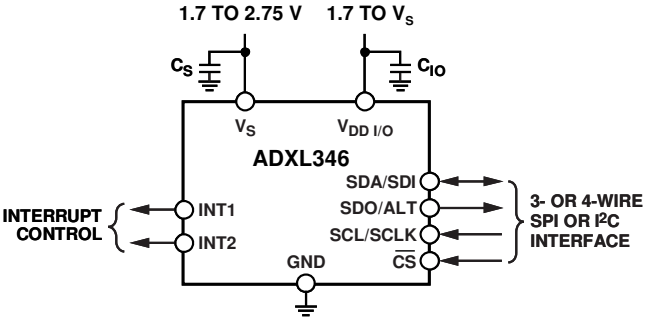

Figure 28. Application Diagram

MECHANICAL CONSIDERATIONS FOR MOUNTING

The ADXL346 should be mounted on the PCB in a location close to a hard mounting point of the PCB to the case. Mounting the ADXL346 at an unsupported PCB location, as shown in Figure 29, may result in large, apparent measurement errors due to undampened PCB vibration. Locating the accelerometer near a hard mounting point ensures that any PCB vibration at the accelerometer is above the accelerometer's mechanical sensor resonant frequency and, therefore, effectively invisible to the accelerometer.

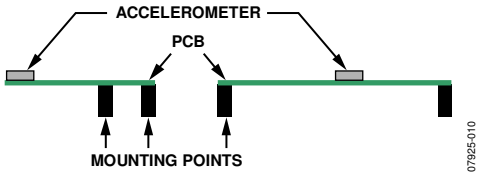

Figure 29. Where Not to Place an Accelerometer

TAP DETECTION

The tap interrupt function is capable of detecting either single or double taps. The following parameters are shown graphically in Figure 30 for a valid single and valid double tap event:

- The tap detection threshold is defined by the THRESH_TAP register (Address 0x10).
- The maximum tap duration time is defined by the DUR register (Address 0x21).
- The tap latency time is defined by the latent register (Address 0x22) and is the waiting period from the end of the first tap until the opening of the time window, which is determined by the value in the window register, for a possible second tap.
- The interval after the latency time (set by the latent register) is defined by the window register. Although a second tap must begin after the latency time has expired, it need not finish before the end of the time defined by the window register.

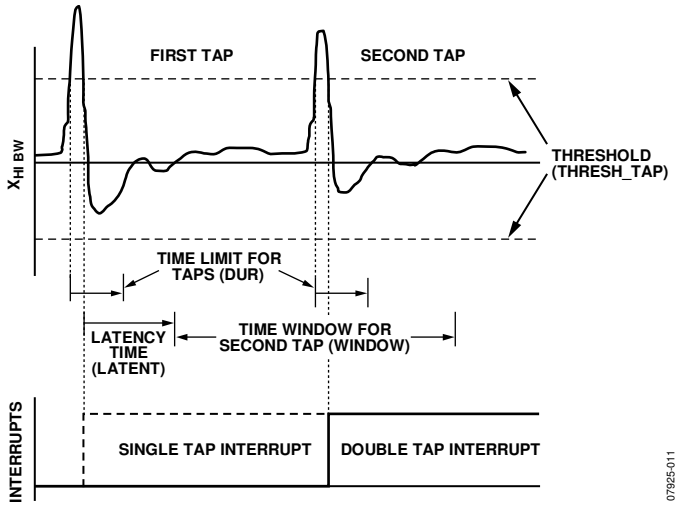

Figure 30. Tap Interrupt Function with Valid Single and Double Taps

If only the single tap function is in use, the single tap interrupt triggers when the acceleration goes below the threshold as long as DUR has not been exceeded. If both single and double tap functions are in use, the single tap interrupt triggers once the double tap event has been either validated or invalidated.

Several events can occur to invalidate the second tap of a double tap event. First, if the suppress bit in the TAP_AXES register is set, any acceleration spike above the threshold during the latency time (set by the latent register) invalidates the double tap detection, as shown in Figure 31.

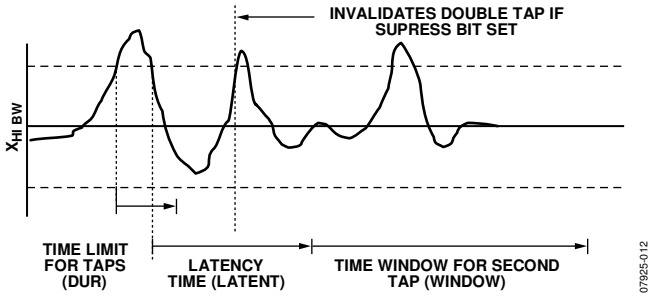

Figure 31. Double Tap Event Invalid Due to High g Event When the Suppress Bit Is Set

A double tap event can also be invalidated if acceleration above the threshold is detected at the start of the time window for the second tap (set by the window register), resulting in an invalid double tap at the start of this window, as shown in Figure 32. Additionally, a double tap event can be invalidated if an acceleration exceeds the time limit for taps (set by the DUR register), resulting in an invalid double tap at the end of the DUR time limit for the second tap event, also shown in Figure 32.

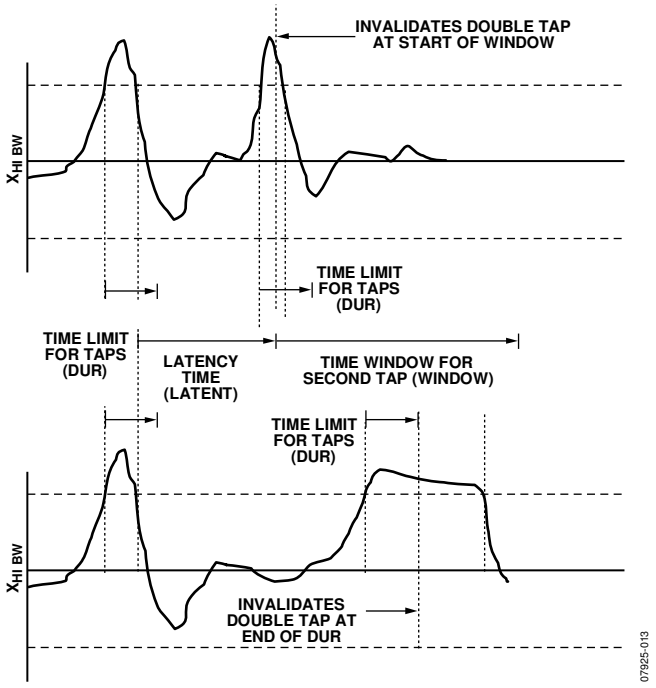

Figure 32. Tap Interrupt Function with Invalid Double Taps

Single taps, double taps, or both can be detected by setting the respective bits in the INT_ENABLE register (Address 0x2E).

Control over participation of each of the three axes in tap/double tap detection is exerted by setting the appropriate bits in the TAP_AXES register (Address 0x2A). For the double tap function to operate, both the latent and window registers must be set to a nonzero value.

Every mechanical system has somewhat different tap/double tap responses based on the mechanical characteristics of the system, so some experimentation with values for the latent, window, and THRESH_TAP registers is required. In general, a good starting point is to set the latent register to a value greater than 0x10, to set the window register to a value greater than 0x10, and to set the THRESH_TAP register to be greater than 3 *g*. Setting a very low value in the latent, window, or THRESH_TAP register may result in an unpredictable response due to the accelerometer picking up echoes of the tap inputs.

After a tap interrupt has been received, the first axis to exceed the THRESH_TAP level is reported in the ACT_TAP_STATUS register. This register is never cleared, but is overwritten with new data.

TAP SIGN

A negative sign is produced by experiencing a negative acceleration, which corresponds to tapping on the positive face of the device for the desired axis. The positive face of the device is the face such that movement in that direction would be positive acceleration. For example, tapping on the face corresponding to the +X direction, labeled Front in Figure 33, would result in a negative sign for the X-axis. Tapping on face labeled Right in Figure 33 would result in a negative sign for the Y-axis and tapping on the face labeled Top would result in a negative sign for the Z-axis. Conversely, tapping on the opposite sides of those described would result in positive signs for the corresponding axes.

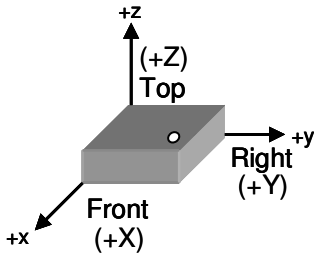

Figure 33. 3-D Orientation with Coordinate System

THRESHOLD

The lower output data rates are achieved by decimation of a common sampling frequency inside the device. The activity, free-fall, and tap/double tap detection functions are performed using unfiltered data. Since the output data is filtered, the high frequency and high *g* data that is used to determine activity, free-fall, and tap/double tap events may not be present if the output of the accelerometer is examined. This may result in trigger events being detected when acceleration does not appear to trigger an event because the unfiltered data may have exceeded a threshold

or remained below a threshold for a certain period of time while the filtered output data has not exceeded such a threshold.

LINK MODE

The function of the link bit is to reduce the number of activity interrupts the processor must service by setting the device to only look for activity after inactivity. For proper operation of this feature, the processor must still respond to the activity and inactivity interrupts by reading the INT_SOURCE register (Address 0x30) and, therefore, clearing the interrupts. If an activity interrupt is not cleared, the part cannot go into auto sleep mode. The asleep bit in the ACT_TAP_STATUS register (Address 0x2B) indicates if the part is asleep.

ORIENTATION SENSING

The orientation function of the ADXL346 reports both 2-D and 3-D orientation concurrently through the ORIENT register (Address 0x3C). The V2 and V3 bits, corresponding to bits D6 and D3 in the ORIENT register, report the validity of the 2-D and 3-D orientation codes. If V2 or V3 are set, their respective code is valid. If V2 or V3 are cleared, the orientation of the accelerometer is unknown, such as when the orientation is within the deadzone between valid regions.

For 2-D orientation sensing, the relation of the x- and y-axes to gravity is used to determine the accelerometer orientation, as shown in Figure 34, with the codes shown in Table 19. Portrait positive corresponds to the x-axis being most closely aligned to the gravity vector and directed upwards, opposite the gravity vector. Portrait negative is the opposite of portrait positive with the x-axis pointing downwards along the gravity vector. Landscape positive corresponds to the y-axis being most closely aligned with the gravity vector and directed upwards, away from the gravity vector. Landscape negative is the orientation opposite landscape positive. The deadzone regions are shown in the orientations for Portrait Positive(+X) and Portait Negative(-X) of Figure 34. These regions also exist for Landscape Positive(+Y) and Landscape Negative(-Y), but are not shown.

In 3-D orientation, the z-axis is also included. If the accelerometer is placed in a Cartesian coordinate system, as shown in Figure 33 of the Tap Sign section, the top of the device corresponds to the positive z-axis direction, the front of the device corresponds to the positive x-axis direction and the right side of the device corresponds to the positive y-axis direction.

The states shown in Table 20 correspond to which side of the accelerometer is directed upwards, opposite the gravity vector. As shown in Figure 33, the accelerometer is oriented in the Top state. If the device was flipped over such that the top of the device is facing down, towards gravity, the orientation would be reported as the Bottom state. If the device is adjusted such that the positive X-axis or positive Y-axis directions were pointing upwards, away from the gravity vector, the accelerometer would report the orientation as Front or Right, respectively.

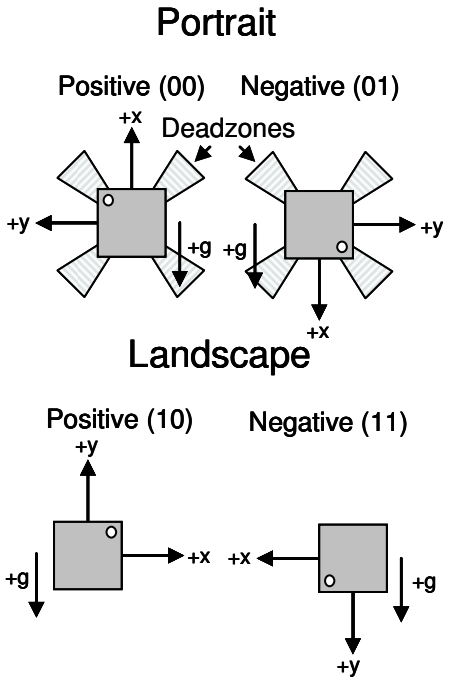

Figure 34. 2-D Orientation with Corresponding Codes

The algorithm to detect orientation change is performed after filtering the output acceleration data to eliminate the effects of high frequency motion. This is performed by using a moving average filter of depth Divisor, set in the ORIENT_CONF register (Address 0x3B). The orientation register is updated at the same rate as the data rate set in the BW_RATE register, but is effectively bandwidth limited to the accelerometer bandwidth divided by Divisor. To eliminate most human motion such as walking or shaking, a Divisor value should be selected to effectively limit the orientation bandwidth to 1 or 2 Hz.

The width of the deadzone region between two or more orientation positions is determined by setting the Deadzone value in the ORIENT_CONF register. The deadzone region size can be specified with a resolution of 3.6°. The deadzone angle represents the total angle where the orientation is considered invalid. Therefore, a deadzone of 10.8° corresponds to 5.4° in either direction away from the bisector of two bordering regions. An example with a d of 10.8° is shown in Figure 35.

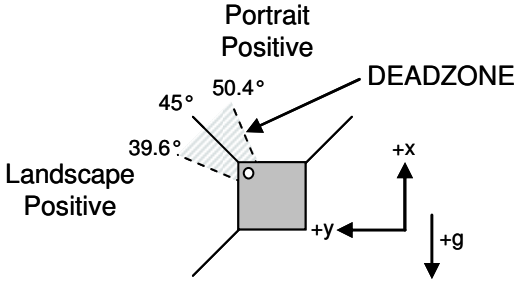

Figure 35. Orientation showing a 10.8° DEADZONE region

LAYOUT AND DESIGN RECOMMENDATIONS

Figure 36 shows the recommended printed wiring board land pattern, and Figure 37 and Table 21 provide details about the maximum rated soldering profile.

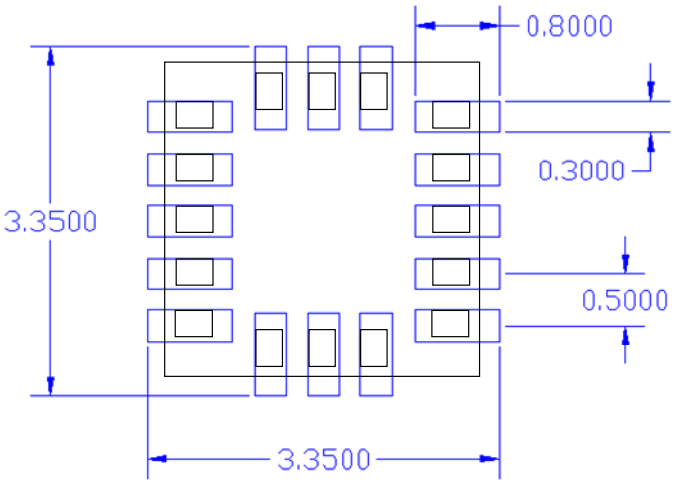

Figure 36. Recommended Printed Wiring Board Land Pattern (Dimensions Shown in Millimeters)

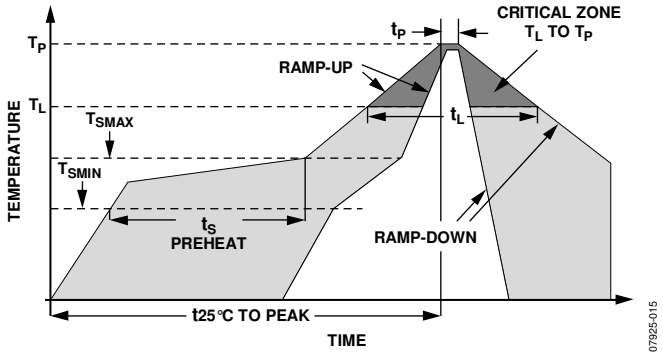

Figure 37. Recommended Soldering Profile

Table 21. Recommended Soldering Profile[1, 2]

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate from Liquid Temperature (T_L) to Peak Temperature (T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time from T_{SMIN} to T_{SMAX} (t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L		
Ramp-Up Rate	3°C/sec max	3°C/sec max
Liquid Temperature (T_L)	183°C	217°C
Time Maintained Above T_L (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240 + 0/−5°C	260 + 0/−5°C
Time of Actual T_P − 5°C (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 minutes max	8 minutes max

[1] Based on JEDEC Standard J-STD-020D.1.
[2] For best results, the soldering profile should be in accordance with the recommendations of the manufacturer of the solder paste used.

OUTLINE DIMENSIONS

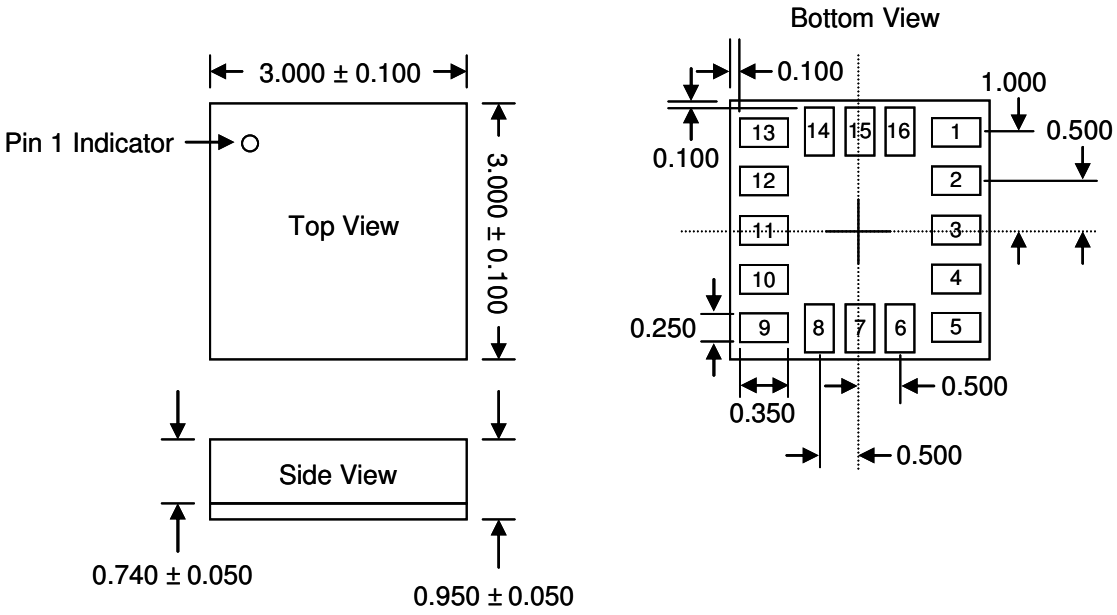

Figure 38. 16-Pin Land Grid Array [LGA] Package
3.00 mm × 3.00 mm Body, Thick Quad
Dimensions shown in millimeters
Lead finish: matte tin

ORDERING GUIDE

Model	Measurement Range (*g*)	Specified Voltage (V)	Temperature Range	Package Description	Package Option
ADXL346BCCZ[1]	±2, ±4, ±8, ±16	2.5	−40°C to +85°C	14-Terminal Land Grid Array Package [LGA]	CC-14-1
ADXL346BCCZ–RL[1]	±2, ±4, ±8, ±16	2.5	−40°C to +85°C	14-Terminal Land Grid Array Package [LGA]	CC-14-1
ADXL346BCCZ–RL7[1]	±2, ±4, ±8, ±16	2.5	−40°C to +85°C	14- Terminal Land Grid Array Package [LGA]	CC-14-1
EVAL-ADXL346Z[1]				Evaluation Board	

[1] Z = RoHS Compliant Part.